

## IN THE CLAIMS

1-12 (Canceled)

13. (Currently Amended) A bipolar junction transistor comprising:
- in a substrate, a first isolation structure spaced apart from a second isolation structure;
  - an epitaxial base layer formed in the substrate;
  - an emitter stack disposed immediately above the epitaxial base layer above the substrate and between the first isolation structure and the second isolation structure, wherein the emitter stack has an emitter stack perimeter;
    - a recess disposed immediately adjacent to the emitter stack and disposed between the emitter stack and the first isolation structure, wherein the recess exposes a collector tap having a collector tap perimeter, wherein the emitter stack and the recess share a boundary, and wherein the emitter stack perimeter and the collector tap perimeter share a co-linear boundary; and
    - an emitter cut provided at the bottom of said emitter stack and immediately on top of an intrinsic base structure formed in epitaxial base layer of the substrate.

14-16 (Canceled)

17. (Original) The bipolar junction transistor according to claim 13, further including:
- a buried layer disposed in the substrate between the first isolation structure and the second isolation structure.
18. (Previously Presented) The bipolar junction transistor according to claim 13, further including:

a collector structure disposed in the substrate below the emitter stack;  
wherein the intrinsic base structure is disposed between the emitter stack and the  
collector structure.

19. (Previously Presented) The bipolar junction transistor according to claim 13, further including:

a collector structure disposed in the substrate below the emitter stack;  
a dielectric layer disposed above the substrate and below the emitter stack; wherein the  
dielectric layer is patterned for said emitter cut to be formed therein and above the collector  
structure; and  
wherein the intrinsic base structure is disposed between the emitter cut and the collector  
structure.

20. (Original) The bipolar junction transistor according to claim 13, further including:  
in the substrate, a collector tap disposed in the recess, wherein the collector tap is selected  
from a P-- collector tap, a P- collector tap, a P collector tap, a P+ collector tap, a P++ collector  
tap, an N-- collector tap, an N- collector tap, an N collector tap, an N+ collector tap, and an N++  
collector tap.

21. (Original) The bipolar junction transistor according to claim 13, wherein the substrate  
includes a bipolar-complementary metal oxide semiconductor (BiCMOS) structure.

22. (Original) The bipolar junction transistor according to claim 13, wherein the BJT is selected from a monojunction BJT device and a heterojunction BJT device.

23-26 (Canceled)

27. (Previously Presented) The bipolar junction transistor according to claim 13, wherein the collector tap is self-aligned.

28. (Previously Presented) The bipolar junction transistor according to claim 13, wherein the bipolar junction transistor is an NPN transistor, and wherein the collector tap is selected from an N-- collector tap, an N- collector tap, an N collector tap, an N+ collector tap, and an N++ collector tap.

29. (Previously Presented) The bipolar junction transistor according to claim 13, wherein the bipolar junction transistor is a PNP transistor, and wherein the collector tap is selected from a P-- collector tap, a P- collector tap, a P collector tap, a P+ collector tap, and a P++ collector tap.

30. (Previously Presented) The bipolar junction transistor according to claim 13, wherein the collector tap has no doping that is different from the substrate.

31. (Previously Presented) The bipolar junction transistor according to claim 13, wherein the recess is a contact corridor.